The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-16. (Canceled)

17. (Currently Amended) A display device comprising:

a display portion;

a first VRAM for storing a first image data;

a second VRAM for storing a second image data;

a comparator circuit for comparing the first and second image data;

a synchronizing signal regulator circuit for ~~selectively outputting~~ controlling a supply of horizontal and vertical synchronizing signals to an LCD controller depending upon an output from the comparator; and

a timer circuit operationally connected to the comparator circuit, wherein said timer circuit starts to count when the first and second image data coincide.

18. (Original) The display device according to claim 17 wherein said display device is a liquid crystal device.

19. (Original) The display device according to claim 17 wherein said synchronizing signal regulator circuit comprises AND circuits.

20. (Currently Amended) A display device comprising:

a display portion;

a first VRAM for storing a first image data;

a second VRAM for storing a second image data;

a comparator circuit for comparing the first and second image data;

a synchronizing signal regulator circuit for ~~selectively outputting~~ controlling a supply of a vertical synchronizing ~~signals~~ signal to an LCD controller depending upon an output from the comparator; and

a timer circuit operationally connected to the comparator circuit, wherein said timer circuit starts to count when the first and second image data coincide.

21. (Original) The display device according to claim 20 wherein said display device is a liquid crystal device.

22. (Original) The display device according to claim 20 wherein said synchronizing signal regulator circuit comprises AND circuits.

23. (Currently Amended) A display device comprising:

a display portion;

at least one video random access memory for storing at least first and second image data;

a comparator circuit for comparing the first and second image data;

a synchronizing signal generator circuit for ~~outputting~~ controlling a supply of a horizontal synchronizing ~~signals~~ signal and a vertical synchronizing ~~signals~~ signal;

a synchronizing signal regulator circuit for receiving an output signal from the comparator circuit and the horizontal and vertical synchronizing signals; [[and]]

a controller operationally connected to the synchronizing signal regulator circuit; and

a timer circuit operationally connected to the comparator circuit, wherein said timer circuit starts to count when the first and second image data coincide.